

**Qualification New Die / Layout
 optimization on L78xx – HBIP40V
 L7805ABV - XA05
 TO220**

General Information		Locations	
Product Line	XA0501	Wafer fab	SINGAPORE Ang Mo Kio
Product Description	1.5 A positive voltage regulators	Assembly plant	SHENZHEN B/E
P/N	L7805ABV	Reliability Lab	Catania
Product Group	AMG	Reliability assessment	Pass
Product division	GENERAL PURPOSE ANALOG & RF		
Package	TO220 - SINGLE GAUGE		
Silicon Process technology	BiP HF		
Process Family	HBIP40V		
Production mask set rev.	LX00C REV A for DIE CODE: PXA		
Maturity level step	30		

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	January 2018	8	Alfio Rao	Giovanni Presti	Final Report
1.1	August 2019	8	Alfio Rao	Sergio Spampinato	Objective review

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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

Qualification of a new die layout optimization for L78xx series (5V, 12V and 15V Output Voltage versions) in HBIP40V Technology.

The change mainly consists in EWS trimming structure removal, resulting in a die size optimization.

In details, the Test Vehicle used for the qualification is L7805ABV - XA05 assembled in TO220 package.

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description



The L78 series of three-terminal positive regulators is available in TO-220, TO-220FP, D²PAK and DPAK packages and several fixed output voltages, making it useful in a wide range of applications. These regulators can provide local on-card regulation, eliminating the distribution problems associated with single point regulation. Each type embeds internal current limiting, thermal shut-down and safe area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over

1 A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltage and currents.

4.2 Construction note

P/N: L7805ABV	
Wafer/Die fab. information	
Wafer fab manufacturing location	SINGAPORE Ang Mo Kio
Technology	BiP HF
Process family	HBIP40V
Die finishing back side	CHROMIUM/NICKEL/SILVER
Die size	1,310, 1,470 micron
Passivation type	P-VAPOX/NITRIDE
Wafer Testing (EWS) information	
Electrical testing manufacturing location	Ang Mo Kio EWS
Tester	ETS300
Test program	XA051B601
Assembly information	
Assembly site	SHENZHEN B/E
Package description	TO220 - SINGLE GAUGE
Molding compound	Epoxy
Frame material	FRAME TO220 SG LCC Ve1 OpE/F3/G3 Bare Cu
Die attach material	Epoxy
Wires bonding materials/diameters	WIRE Cu D2 BL40-55g EL15-25% 500m
Final testing information	
Testing location	SHENZHEN B/E
Tester	QT200
Test program	XL05_01.cts #FA05

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Diffusion Lot	Assy Lot	Technical Code	Package	Product Line	Part number
1	V6723T4T	GK7360VD	V3)K*XA051B6	TO220 - SINGLE GAUGE	XA05	L7805ABV

5.2 Test plan and results summary

P/N: L7805ABV

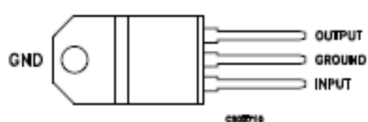
Part: L7669ADV

Test		Std ref.	Conditions	SS	Steps	Failure/SS Lot 1	Note
Die Oriented Tests							
HTOL		JESD22 A-108	T _j = 125°C, BIAS 35 V	77	168 h	0/77	
		500 h			0/77		
		1000 h			0/77		
HTSL		JESD22 A-103	T _a = 150°C	45	168 h	0/45	
		500 h			0/45		
		1000 h			0/45		
Package Oriented Tests							
AC		JESD22 A-102	Pa=2Atm / Ta=121°C	77	168 h	0/77	
TC		JESD22 A-104	T _a = -65°C to 150°C	77	100 cy	0/77	
	200 cy				0/77		
	500 cy				0/77		
THB		JESD22 A-101	T _a = 85°C, RH = 85%, BIAS 24 V	77	168 h	0/77	
	500 h				0/77		
	1000 h				0/77		
Other Tests							
ESD		JESD22-A114	HBM	3	+/-2000V	Pass	
		JESD22-C101	CDM	3	+/-500V	Pass	

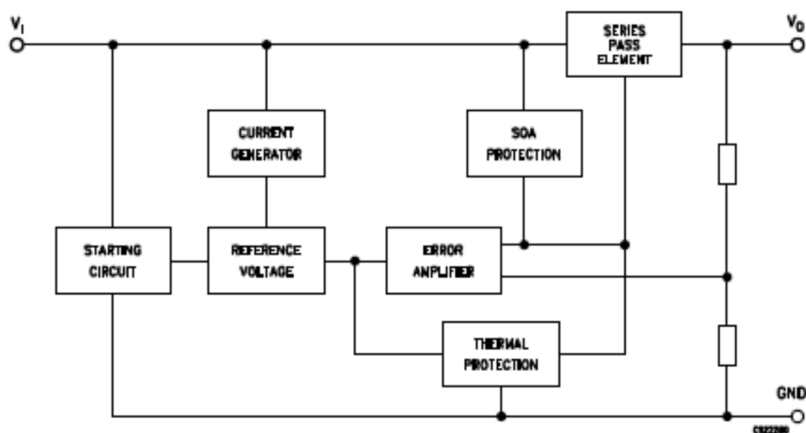
6 ANNEXES

6.1 Device details

6.1.1 Pin connection



6.1.2 Block diagram



6.2 Tests Description

Test name	Description	Purpose
Die Oriented		
HTOL High Temperature Operating Life	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
Package Oriented		
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
Other		
ESD Electro Static Discharge	The device is submitted to a high voltage peak on all his pins simulating ESD stress according to different simulation models. CDM: Charged Device Model	To classify the device according to his susceptibility to damage or degradation by exposure to electrostatic discharge.